CLAIMS

1. A method of fabricating a non-volatile memory device having a tunnel insulating layer, comprising:

sequentially depositing said tunnel insulating layer, a conductive layer, and a first insulating layer over a semiconductor substrate, said tunnel insulating layer including at least two portions of different thicknesses;

selectively etching the resultant structure to a given depth to form trenches;

depositing a second insulating layer over said structure including said trenches;

selectively removing said second insulating layer so as to form element isolation regions composed of the trenches filled with said second insulating layer;

removing said first insulating layer; and

selectively removing said second insulating layer using a chemical mechanical polishing (CMP) process until said conductive layer is exposed, the conductive layer being used as a stopping layer for the CMP process.

2. A method as defined in Claim 1, wherein said conductive layer serves as a floating gate in a transistor device formed as part of a memory cell in the memory device.

3. A method as defined in Claim 1, wherein said conductive layer has a thickness of 50 to 1000Å.

4. A method as defined in Claim 1, wherein said first insulating layer is formed of a material selected from the group consisting of SiN, BN, and CN.

5. A method as defined in Claim 1, wherein said first insulating layer has a thickness of 100 to 1000Å.

6. A method as defined in Claim 1, wherein the step of selectively removing said second insulating layer comprises:

subjecting said structure to photolithography to selectively etch said second insulating layer;

flattening said first and second insulating layers through a CMP process;

performing photolithography to selectively remove the flattened first insulating layer; and

subjecting said second insulating layer to a CMP process to complete said element isolation regions.

7. A method as defined in Claim 6, wherein the step of selectively removing said flattened first insulating layer is performed until said conductive layer is exposed.

8. A method as defined in Claim 1, wherein said second insulating layer is formed of a material selected from the group consisting of HDP, BPSG, SOG, Fox, USG, HOSP, and black diamond.

9. A method as defined in Claim 1, wherein the step of selectively removing said second insulating layer by the CMP process employs a slurry with selectivity between said second insulating layer and the conductive layer equal to or greater than 1.